REMARKS/ARGUMENTS

Prior to this amendment, claims 1-32 were pending. In this amendment, claims 1-14 and 26-32 are amended. No claims are canceled and claims 33-35 are added. No new matter is added. Thus, after entry of this amendment, claims 1-35 will be pending.

Claim Rejections - 35 USC § 101, non-statutory subject matter

Claims 1-32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1 and 26

The Office Action states that claims 1 and 26 are directed to an apparatus; however, the claimed limitations appear to be software per se, as the unit can be interpreted to be merely software. Thus the claims are lacking any structural or hardware components comprising the apparatus.

It is not clear what test or section of the MPEP the Office Action is using for this rejection. Applicants note that the test requiring a "practical application" that provides a "tangible, concrete, and useful result" is no longer a valid test to be employed in determining whether or not a claim is directed to statutory subject matter. *In Re Bilski*, U. S. Court of Appeals for the Federal Circuit 2007-1130 (Serial No. 08/833,892), page 20.

Claim 1 recites a "multiplication circuit" comprised of hardware components, such registers, a multiplier, and accumulation units. Thus, claim 1 is directed to a machine (i.e. a circuit).

The remaining valid test for determining the patentability for a machine is whether the claims would have the practical effect of patenting only a law of nature, a natural phenomenon, or an abstract idea, such as a formula. *Id.*, page 9.

Claim 1 would not wholly pre-empt a mathematical formula for multiplying two numbers because claim 1 is directed to a particular apparatus for performing multiplications in a particular manner, not in any manner. For example, claim 1 recites a multiplication circuit having a particular configuration of registers connected via specific inputs to a multiplier, which is then connected to accumulation units. The registers and accumulation units are also of

particular sizes. The modes of the multiplication circuit use these circuit elements to operate in a particular manner.

Thus, claim 1 does not pre-empt any fundamental principles of multiplying two numbers, but is directed to a particular circuit to perform different types of multiplication in a specific manner.

Accordingly, claims 1 and 26 are directed to patentable subject matter.

Claim 14

Recently, the Federal Circuit has clarified the only test for determining whether a method claim is directed to statutory subject matter. "A claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." *Id.,* page 10.

Claim 14 is directed to a particular machine or apparatus, as is described above. As to what satisfies (1), the Federal Circuit stated "a claim that is tied to a particular machine ... does not pre-empt all uses of a fundamental principle in any field but rather is limited to a particular use, a specific application." *Id.,* page 16.

For a same reason as described above, claim 14 does not pre-empt all uses of a fundamental principle.

Accordingly, claim 14 is directed to patentable subject matter.

Claim Rejections - 35 USC § 112, first paragraph

Claims 1-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement regarding the claim element "...without summing any intermediate results." This clam term is no longer recited. Accordingly, Applicants respectfully request withdrawal of this rejection.

Claim Rejections - 35 USC § 103(a) Moyse, Yu, Lee, Henderson, Bosshart

Claims 1-6, 1 1-1 9, 24-27, and 31 -32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyse (US Pat. 5,446,651) in view of Yu (6,523,055) and Lee et al. (hereafter Lee)(US Pat. 5,579,253).

Claim 1

Claim 1 is allowable over these cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *in the first mode for multiplying two N-bit numbers,*
> *a first long word length multiplicand is formed at the first 2N-bit input from a first short word length multiplicand stored in the first register,*
> *a second long word length multiplicand is formed at the second 2N-bit input from a second short word length multiplicand stored in the second register, and*
> *the first and second long word length multiplicands are multiplied together using the 2N-bit multiplier to form a 4N-bit result that includes the product of the first and second short word length multiplicands; and*
> *in the second mode for multiplying two 2N-bit numbers,*
> *a third long word length multiplicand is formed at the first 2N-bit input from a first pair of short word length words, wherein a first word of the first pair is stored in the first register,*
> *a fourth long word length multiplicand is formed at the second 2N-bit input from a second pair of short word length words, wherein a first word of the second pair is stored in the second register, and*
> *subsequently the third and fourth long word length multiplicands are multiplied together using the 2N-bit multiplier to form a 4N-bit result.*

In Moyse, there are two modes. *See Moyse*, col. 5 lines 27-29. A 2N by 2N multiplication mode (asserted second mode) multiples two 2N bit numbers to create a 4N bit product. *Id.*, col. 5 lines 39-41. An N by N multiplication mode (asserted first mode) multiplies N bit numbers to obtain a 2N bit product, not a 4N bit product. *Id.* There are two separate 2N bit products, but not one 4N bit product. Accordingly, the proposed combination does not teach or suggest "*the first and second long word length multiplicands are multiplied together using the 2N-bit multiplier to form a 4N-bit result that includes the product of the first and second short word length multiplicands*," as recited in claim 1.

Additionally, the Office Action states that Yu discloses "a multiplier circuit in which multiplicands generate intermediate products wherein sign extension and zeroing are performed to properly align inputs for multiplication." (emphasis added). The Office Action

then asserts that this teaching would be used to extend each N bit number into a 2N bit number in the N by N multiplication mode.

However, in Moyse's N by N multiplication mode, a data word is composed of two N bit numbers. *Id.*, col. 5 lines 32-39. Thus, extending the length of one N bit number to create a 2N bit number would erase the other N bit number in the data word. This would then destroy the stated functionality of the N by N multiplication mode, which is to multiply two pairs of N bit numbers. *Id.*, col. 5 line 28.

Additionally, Yu teaches extending the sign of an intermediate product, not an input to a multiplication circuit. Thus, even if Yu could be combined with Moyse, the combination would provide an extension of a partial product, not of an input to a multiplier. Accordingly, the proposed combination does not teach or suggest "*a first long word length multiplicand is formed at the first 2N-bit input from a first short word length multiplicand stored in the first register*," as recited in claim 1.

For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

Claims 14 and 26

Applicants submit that independent claims 14 and 26 and their respective dependent claims are allowable for a same reason as claim 1.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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